Carbon nanotube for nanoelectronics

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Abstract-Issues for realizing carbon nanotube nanoelectronics have been discussed. The main issues are selective growth and electron energy bandgap engineering, which can be controlled by CNTs' diameter, chirality, and surface functionalization. We have introduced nanotemplate to control selective growth, length and diameter of CNT. Ohmic contact of the CNT/metal interface was formed by rapid thermal annealing (RTA). Diameter control and surface modification of CNT open the possibility to energy band gap modulation. A type of CNT-nonvolatile memory based on the top gate structure with oxide-nitride-oxide charge trap is presented in this paper.

Introduction

Carbon nanotube (CNT) is one of the candidates for a quantum wire for the molecular-FET. CNTs show exceptional electronic and mechanical properties together with its nano-size diameter and hollowness. They behave like one-dimensional quantum wires that can be either metallic or semiconducting, depending on their chirality and diameter [1]. It is also expected that the CNTs could solve the thermal dissipation problem due to their high thermal conductivity. CNTs can transport terrific amount of electric current without considering doping problem in Si-FETs because the bonds among carbon atoms are much stronger than those in any metal. Recently, several papers have been reported on the CNTs for FETs and CNT-logic applications [2]. However, obstacles still remain for device realization, such as aligning CNTs and controlling quality (energy band gap) of CNTs.

Selective Growth of CNT

The future integration with conventional microelectronics as well as development of novel devices requires that CNTs can be grown in highly ordered arrays or located at a specially defined position such as predeposited catalyst pads or partially exposed nano template. In order to get highly ordered CNTs in the selective area, anodic aluminum oxide (AAO) template was employed. Diameter, thickness, and length of CNT are changed by controlling geometry of AAO template. Thickness of CNT is controlled by changing density of reaction gases as shown in Fig. 2. Diameter and length of nano holes are controlled by changing applied voltage, bias-time and type of solution. (Fig. 1). [3].

A vertically aligned transistor is fabricated in the following steps: nano-pore formation by anodization, CNT synthesis, metal-electrode formation, oxide deposition and patterning, gate electrode formation [4]. A transistor can be constructed as small as the diameter of the CNT. The SiO_2 was deposited at the top of aligned CNTs and followed by e-beam patterning, so that the electrode attached to the CNTs only through the patterned holes. The gate oxide of SiO_2 was deposited followed by deposition of top gate electrode. The transistor unit cell can be achieved as small as the diameter of CNT, which corresponds to the tera-level CNT transistor with a density of 10^{12} element per square centimeter.

Fig. 3 shows SEM images of selectively grown carbon nanotube arrays which have been ion milled to remove residual amorphous carbon from the template surface and then partially exposed by etching the alumina matrix using a mixture of phosphoric and chromic acid. In the integrated device, each CNT is electrically attached to the bottom electrode (row) and upper electrode (column), and the gate electrode is positioned over the top electrode. Each cross point of two electrodes, bottom and upper, corresponds to a device element with a single vertical CNT. The gate metal is deposited right after the oxide deposition over the drain electrode. The speed of the ON / OFF switch depends on the frequency of array sweeping, in which the ON state corresponds to where both the cross-point and gate electrodes are turned on [5].

We modified shape of CNTs by introducing AAO nano template, where the Y-shape nano holes are formed during AAO fabrication. The measured resistance of Y-shape CNTs is increased, which is attributed the hetero-junction formation due to the different diameter [Fig 4].

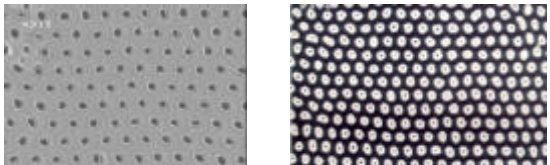

Figure 1. SEM images of vertically grown carbon nanotube with different thickness.

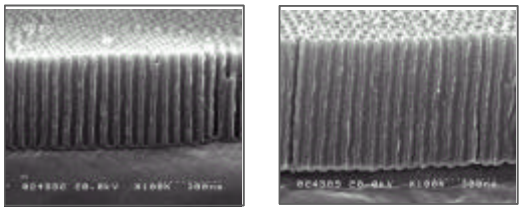

Figure 2. SEM images of aluminum anodized oxide nanotemplate with different length of 500nm and 1000nm respectively.

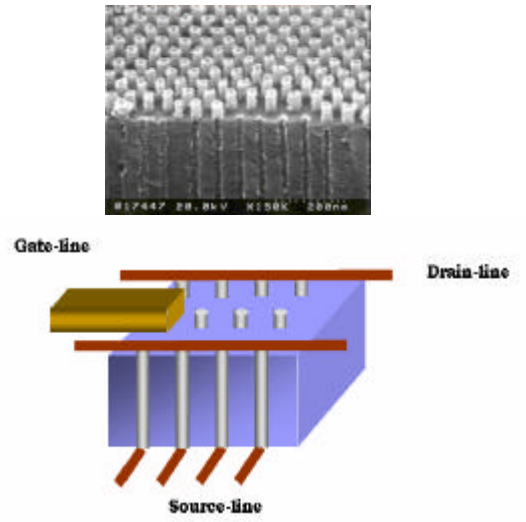

Figure 3. SEM image of vertically aligned CNTs (upper), and device architecture of vertical CNT-transistor array (lower).

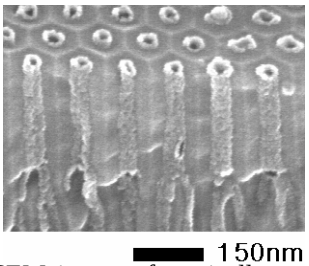

Figure 4. SEM image of vertically grown Y-shape carbon nanotube array.

Ohmic contact of CNT/electrode is required for the carbon nanotube based FET device operation. In order to improve the contact property of CNT/metal, rapid thermal annealing (RTA) process was performed. The carbide formation during RTA process may attribute to enhance contact property and thus make ohmic contact. IV characteristic of RTA treated CNTs as a function of annealing temperature is shown in Fig. 5. The conductance (dI/dV) was increased from 30 mS at the RTA temperature of 500 ºC to 50 mS at 800 ºC.

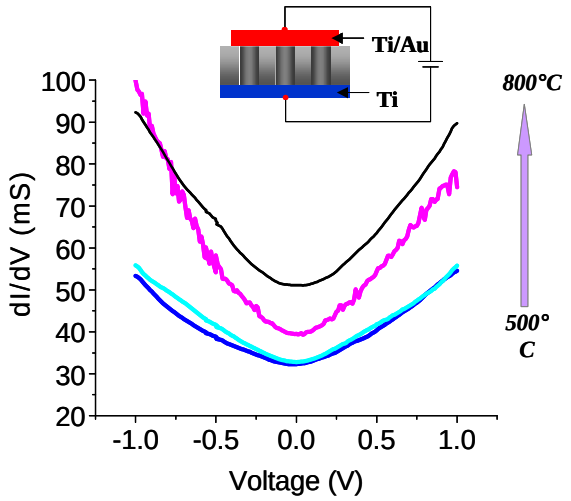

Figure 5 Conductance of rapid thermal annealed CNT as a function of annealing temperature.

Carbon nanotube FET

Carbon nanotube-based field effect transistor (CNT-FET) has been reported either by employing a back gate electrode or by a top gate electrode on top of a silicon wafer covered with an oxide. The CNTFET typically exhibit p-type characteristics under ambient condition due to the adsorbed oxygen molecules. The improved electrical properties in terms of I-V behavior and transconductance were achieved by employing a thin gate oxide with the top gate structure. The transconductance and I_{on}/I_{off} ratio was 2321μS/μm and ~$2x10^4$ respectively [3]. Fig. 6 shows the output characteristic for a CNT-FET with top gate and an oxide layer of 28nm [6]. The CNT is passivated by oxide film so that atmosphere does not influence on the electrical transport property of CNT as compared to previously reported results. The device shows p-type CNT-FET behavior where current increases with increasing negative gate voltage, whereas decreases down to a few femto ampere (fA) range with positive gate voltages. I_{on}/I_{off} ratio is over 10^5 at 1V of V_{sd} while gate voltage was sweeping from -4V to 4V in contrast with the off-state current was kept at less than a few pA. The low off-state current would be attributed to the geometry of top gate electrode and a high quality of oxide film. The operating temperature of CNT-FET is dependent on the energy bandgap of

CNTs, which is directly related with the way to make CNTs. Higher performance of CNTFET is expected either by using higher quality of CNTs and by reducing gate oxide thickness.

Carbon nanotube nonvolatile memory

CNTs could be used not only as a switching device and wires for interconnect, but also as a non-volatile memory device. A charge storage node, consisting of oxide-nitride-gate oxide (ONO) is located between CNT and gate electrode. The memory node is deposited onto the CNT followed by deposition of top gate electrode. The Si_3N_4 film is known to contain a large number of charge traps, and thus it provides a low-potential site for storing charges. The measured drain current as the gate voltage was swept up and down revealed clear hysteresis (Fig. 7). The threshold voltage shift is about 2V when the gate sweeping voltage is at 12V. This result suggests that the nonvolatile memory based on CNT channel will be possible.

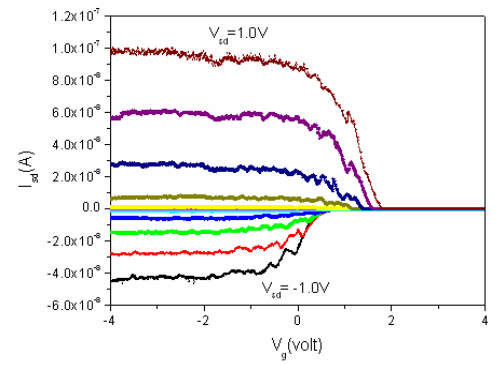

Figure 6 Drain current vs. gate voltage of a CNT-FET.

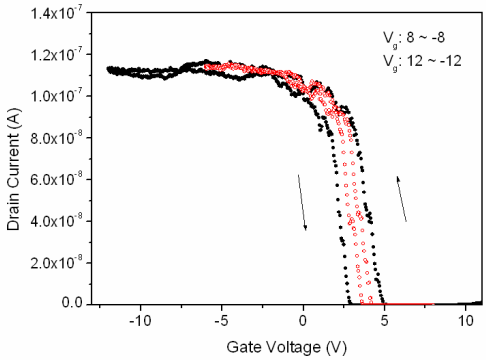

Figure 7 Drain current as a function of gate voltage and source-drain bias of -0.9V.The maximum applied gate voltage in a sweep loop is 8 V and 12V.

The device was characterized by measuring threshold voltage shift after charging the ONO film (the threshold voltage defined as the gate voltage at which the current reaches 5nA) (Fig. 8). The applied positive gate voltage increases the threshold voltage indicating that holes are injected from CNT to the ONO film, so that trap sites are occupied by holes. For 0 to 7V charging voltage pulses, the shift in threshold voltage was found to be quasi- quantized with an increment of 60 mV. The localized charge distribution may be induced in the nitride layer due to the localized high field distribution of CNT. This result suggests that each trap site containing charge in ONO layer of the CNT memory acts like a quantum dot for flash-memory.

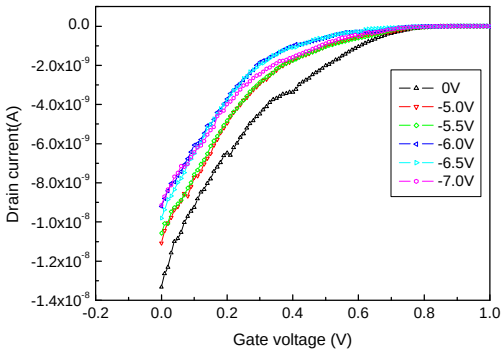

Figure 8 Drain current vs. gate voltage of a CNT-memory after charging the ONO storage node. (pulse=100msec, applied voltage=0 ~ 7V while the drain was maintained at -0.9V).

Acknowledgments

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